



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Dennis Wendell  
Assignee: Sun Microsystems, Inc.  
Title: Low Impedance Memory Bitline Eliminating Precharge  
Serial No.: 10/779,327 Filed: February 13, 2004  
Examiner: Unknown Group Art Unit: Unknown  
Docket No.: SUN040316 Customer No.: 33438

Austin, Texas  
May 13, 2004

COMMISSIONER FOR PATENTS  
PO Box 1450  
Alexandria, VA 22313-1450

### INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. § 1.56, § 1.97 and § 1.98, Applicants wish to call the following documents to the attention of the Examiner.

A PTO form 1449 listing these documents is enclosed.

Citation of the above documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;
2. a representation that a search has been made, other than as described above; or
3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

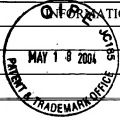
I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: COMMISSIONER FOR PATENTS, PO Box 1450, Alexandria, VA 22313-1450, on May 13, 2004.

*Gary W Hamilton* 5/13/04  
Attorney for Applicant(s) Date of Signature

Respectfully submitted,

*Gary W Hamilton*

Gary W. Hamilton  
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Reg. No. 31,834

U.S. Department of Commerce, Patent and Trademark Office						Attorney Docket No.		Serial No.	
						SUN040316		10/779,327	
						Applicant(s)			
(Use several sheets if necessary)						Dennis Wendell			
						Filing Date		Group	
						February 13, 2004		Unknown	
U.S. Patent Documents									
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate		
	AA	6,667,921	12/23/2003	Park	365	203			
	AB	6,643,804	11/04/2003	Aipperspach et al.	714	718			
	AC	5,963,494	10/05/1999	Khang	365	203			
	AD	5,883,845	03/16/1999	Khang	365	203			
	AC	5,875,139	02/23/1999	Semi	365	203			
	AF	5,848,015	12/0/1998	Seno	365	203			
	AC	5,563,831	10/08/1996	Ting	365	189.09			
	AH	5,007,023	04/09/1991	Kim et al.	365	203			
	AI								
	AJ								
	AK								
Foreign Patent Documents									
		Document	Date	Country	Class	Subclass	Translation		
	AF						Yes	No	
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	AN						<input type="checkbox"/>	<input type="checkbox"/>	
	AD						<input type="checkbox"/>	<input type="checkbox"/>	
	AF						<input type="checkbox"/>	<input type="checkbox"/>	
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)									
	AR	Bhutani, S., et al., "Processor Having a Coalescing Cache Disable Mode," U.S. Patent Application Serial No. 10/766,745, filed January 27, 2004							
	AS	Heald, R., et al., "A Third-Generation SPARC V9 64-b Microprocessor," IEEE JSSC, Nov. 2000, pp. 1526-1538							
	AT	Konstadinidis, G., et al., "Implementation of a Third-Generation 1.1GHz 64b Microprocessor," 2002 IEEE International Solid-State Circuits Conference, Session 20/Microprocessors/20.3							
	AU	Konstadinidis, G., et al., "Implementation of a Third-Generation 1.1GHz 64b Microprocessor," 2002 IEEE Journal of Solid-State Circuits, Vol. 37, No. 11, Nov. 2002, pp. 1461-1469							
Examiner			Date Considered						
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.									

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT						Applicant(s)			
(Use several sheets if necessary)						Dennis Wendell			
						Filing Date		Group	
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U.S. Patent Documents							
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	AA						
	AB						
	AE						
	AD						
	AE						
	AE						
	AG						
	AH						
	AI						
	AI						
	AK						

Foreign Patent Documents								
		Document	Date	Country	Class	Subclass	Translation	
							Yes	No
	AE						<input type="checkbox"/>	<input type="checkbox"/>
	AM						<input type="checkbox"/>	<input type="checkbox"/>
	AN						<input type="checkbox"/>	<input type="checkbox"/>
	AD							
	AP							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)		
	AR	McCarroll, B., et al., "A High-Speed CMOS Comparator for Use in an ADC," IEEE JSSC, Feb. 1988, pp. 159-165
	AS	Wendell, D., et al., "A 4 MB On-Chip L2 Cache for a 90nm 1.6GHz 64 bit Microprocessor," IEEE JSSC, Feb. 2004
	AT	
	AU	

Examiner	Date Considered
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